REMARKS

Claims 1-14 were examined and reported in the Office Action. Claims 1, 2 and 8-14 are rejected. Claims 8-14 are cancelled. Claims 1 and 3 are amended. Claims 1-7 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. Double Patenting

The Office Action states that claims 8-14 are objected to under 37 C.F.R. 1.75 as being a substantial duplicate of claims 1-7. Applicant has canceled claims 8-14 without prejudice.

II. 35 U.S.C. § 102(e)

It is asserted in the Office Action that claims 1-2, 8-9 are rejected under 35 U.S.C. § 102(e), as being anticipated by U.S. Patent No. 6,768,690 issued to Kwon et al ("Kwon"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant has canceled claims 8-9. Therefore the 35 U.S.C. § 102(e) rejection regarding claims 8-9 is moot.

According to MPEP §2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "[a] delay locked loop (DLL) block to generate a delay locked clock signal by delaying an external clock signal in a semiconductor device, comprising: a clock buffer to receive the external clock signal and an inverted signal of the external clock signal to generate a plurality of internal clock signals; a clock divider to receive one of the internal clock signals and a control signal based on a column address strobe (CAS) signal to generate a plurality of divided signals, each having a predetermined pulse width adjusted by the control signal, and output a selected divided signal as the divided signal; and a DLL circuit to receive the plurality of internal clock signals and the divided signal to generate the delay locked clock signal."

In Applicant's claimed invention the clock divider generates a divided signal where each portion has a different pulse width according to the column address strobe (CAS) latency. Since the CAS latency changes according to operational frequency, the pulse width of the divided signal is adjusted according to the operational frequency. Therefore, the delay locked loop (DLL) (including the divided signal) can be operated both at a high operational frequency and a low operational frequency.

Kwon discloses a register controlled delay locked loop (DLL)that reduces current consumption by operating the DLL when a semiconductor device is only in an operation mode. Kwon discloses a clock divider 43 illustrated in Figure 4 does not generate a plurality of divided clock signals. That is, the clock divider disclosed by Kwon only generates one divided clock signal in response to a control signal based on CAS latency. Therefore, Kwon does not teach, disclose or suggest "...a clock divider to receive one of the internal clock signals and a control signal based on a column address strobe (CAS) signal to generate a plurality of divided signals, each having a predetermined pulse width adjusted by the control signal, and output a selected divided signal as the divided signal; and a DLL circuit to receive the plurality of internal clock signals and the divided signal to generate the delay locked clock signal."

Therefore, since Kwon does not disclose, teach or suggest all of Applicant's amended claim 1 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Kwon. Thus,

Applicant's amended claim 1 is not anticipated by Kwon. Additionally, the claims that directly or indirectly depend from claim 1, namely claims 2-3, are also not anticipated by Kwon for the same reasons.

Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejection for claims 1-2 and 8-9 is respectfully requested.

III. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-7, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-7 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: June 6, 2005

By: _____
Steven Laut, Reg. No. 47,736

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on June 6, 2005.

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Jean Svoboda